UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,746	12/11/2001	Matthias Eichin	4284	6354

21553 7590 09/09/2004

FASSE PATENT ATTORNEYS, P.A.
P.O. BOX 726
HAMPDEN, ME 04444-0726

EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,746	EICHIN ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23,25,29,30,33 and 34* is/are rejected.

7)☒ Claim(s) *24,26-28,31,32,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Invention II, claims 21-36 in the reply filed on Sept. 25, 2003 is acknowledged.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 21-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Habersetzer et al (6160413) in view of Chai et al (6046947).

Regarding claim 1, Habersetzer et al disclose [see Fig. 1] a method of testing an integrated circuit (IC 10) comprising the steps: a) providing at least one output signal [shown by down arrow ↓ of operational circuitry 12] generated by a circuit unit (operational circuitry 12) of said integrated circuit (10) to at least one signal output pin (output pins 18) of said integrated circuit (10) during a normal operating mode; d) dependent on and responsive to a result of said evaluating, switching from said normal operating mode [using operational circuitry 12] into a test mode [using test circuitry 14]; and e) during said test mode [using test circuitry 14], generating in said circuit unit (12) at least one test signal [shown by ↔ between operational circuitry 12 and test circuitry 14] that is to be tested, and proving said at least one test signal (↔) to at least one chosen output pin (18) among said at least one signal output pin (18). However, they do not disclose applying an externally applied potential to at least one selected output pin as claimed. Chai et al disclose [see Fig. 1] a method of testing an integrated circuit comprising externally applying an externally applied potential (Vdd) [see col. 2, lines 18-21] to at least one selected one-signal output pin (output driver 14). Further, Chai et al teach that the addition of externally applying an externally applied potential to selected output pin is advantageous because it is able to provide a potential value in order to test a large number of devices simultaneously in a testing apparatus during test mode operation. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Habersetzer et al by adding an externally applied potential as taught by Chai et al in order to be able to provide a potential value for the purpose to test a large number of devices simultaneously in a testing apparatus during test mode operation.

Regarding claim 22, Chai et al disclose connecting a passive circuit (pass gate buffer 32) component to said at least one selected output pin (output driver 14) and generating said externally applied potential through said passive circuit component (32).

Regarding claim 23, Chai et al disclose connecting said passive circuit component (32) between said at least one selected output pin (14) and a reference potential (Vdd).

Regarding claim 25, Habersetzer et al disclose said at least one selected output pin (18) in said step b) and said at least one chosen output pin (18) in said step e) both comprise the same output pin (18) among said at least one signal output pin (18).

Regarding claim 29, Habersetzer et al disclose said circuit unit (12) comprises plural circuit blocks [see Fig. 2], and further comprising respectively activating [via re-enable circuit 26] and deactivating [via disable circuit 24] different ones of said circuit blocks dependent on and responsive to a result of said evaluating.

Regarding claim 30, Habersetzer et al disclose wherein said steps d) and e) are carried out at a time separate from said steps b) and c), and not overlapping with said steps b) and c) [via timing circuit 34].

Regarding claim 33, Habersetzer et al disclose wherein said evaluating in said step c) comprises performing a logical operation [via control logic 32] on said potential value and a signal value of said at least one output signal (18) generated by said circuit unit (12).

Regarding claim 34, Habersetzer et al disclose wherein said step d) switches into said test mode [via test circuitry 14] only when said signal value is zero and said potential value lies in a prescribed potential value range.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Whetsel (5847561), McClure (6037792), and Habersetzer et al (6255838, & 6570400, 6646459) disclose a method and apparatus for integrated circuit (IC) testing.

7. Claims 24, 26-28, 31-32 and 35-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 24, it would not be obvious to one of ordinary skill in the art to have a passive circuit component comprising a resistor in the prior art since the prior art passive circuit component is a tri-state buffer.

Regarding claim 26, primary reason for the allowance of the claim is due to the fact of a method of testing an IC having a first output pin and a second output pin that is distinct and separate from said first output pin.

Regarding claim 27, primary reason for the allowance of the claim is due to the fact of a method of testing an IC providing said first test signal and determine that said externally applied potential has said first potential value, and providing said second test signal to said chosen output pin dependent on and responsive to said evaluating in said step determining that said externally applied potential has said second potential value. Since claim 28 depends from claim 27, it also has allowable subjected matter.

Regarding claims 31-32, primary reason for the allowance of the claim is due to the fact of a method of testing an IC comprises comparing said potential value to at least one reference

value range defined by an upper reference value and a lower reference value, so as to determine whether said potential value falls in said reference value range.

Regarding claim 35, primary reason for the allowance of the claim is due to the fact of a method of testing an IC comprises determining whether said potential value lies within a voltage interval of a voltage window discriminator, and switches into said test mode only when said potential value does lie within said voltage interval of said voltage window discriminator. Since claim 36 depends from claim 35, it also has allowed subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (517) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH

September 3, 2004